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(54) Semiconductor memory device and its manufacturing method

(57) A semiconductor dynamic memory device comprising: a source diffusion layer (6) formed on a semiconductor substrate and connected to a fixed potential line; a plurality of columnar semiconductor layers (2) arranged in a matrix form and formed on the source diffusion layer and each having one end connected to the source diffusion layer commonly, the columnar semiconductor layer taking a first data state with a first threshold voltage that excessive majority carriers are accumulated in the columnar semiconductor layer, and a second data state with a second threshold voltage that excessive majority carriers are discharged from the columnar semiconductor layer; a plurality of drain diffusion layers (5) each formed at the other end of the columnar semiconductor layer; a plurality of gate electrodes (4) each opposed to the columnar semiconductor layer via a gate insulating film, and connected to the word line; a plurality of word lines (9) each connected to corresponding the gate electrodes; and a plurality of bit lines (8) each connected to corresponding the drain diffusion layers, the bit lines being perpendicular to the word lines.

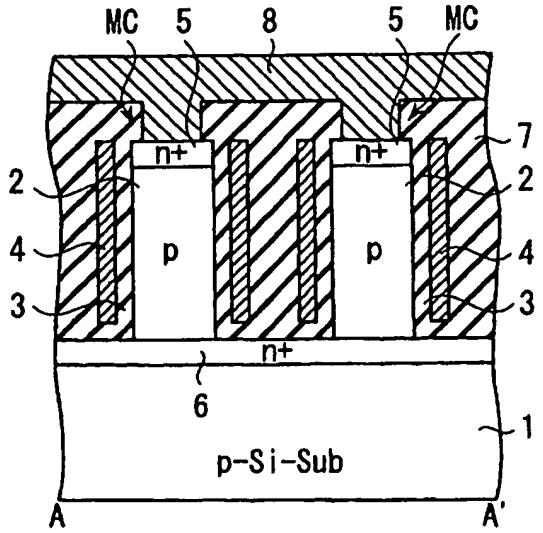

FIG. 2

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cell array according to the same embodiment;
Fig. 23 is a cross-sectional view taken along the B-B' line of Fig. 22;
Fig. 24 is a cross-sectional view taken along the A-A' line of Fig. 22;
Fig. 25 is a diagram of the same DRAM cell array under its manufacturing process;
Fig. 26 is a diagram of the same DRAM cell array under its manufacturing process;
Fig. 27 is a diagram of the same DRAM cell array under its manufacturing process;
Fig. 28 is a diagram of the same DRAM cell array under its manufacturing process;
Fig. 29 is a diagram of the same DRAM cell array under its manufacturing process;
Fig. 30 is a perspective of the structure obtained through the process of Fig. 28;
Fig. 31 is a diagram that shows a memory cell structure according to a still further embodiment;
Fig. 32A is a plan view that shows a pretreatment process of a substrate according to the same embodiment;
Fig. 32B is a cross-sectional view taken along the A-A' line of Fig. 32A;
Fig. 33A is a plan view that shows a pretreatment process of a substrate according to the same embodiment;
Fig. 33B is a cross-sectional view taken along the A-A' line of Fig. 33A;
Fig. 34 is a plan view of a DRAM cell array according to the same embodiment;
Fig. 35A is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 35B is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 36A is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 36B is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 37A is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 37B is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 38A is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 38B is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment;
Fig. 39A is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment; and
Fig. 39B is a cross-sectional view taken along the A-A' line of Fig. 34 to show a manufacturing process of the same embodiment.

DETAILED DESCRIPTION OF THE INVENTION

[0006] Embodiments of the invention will now be explained below with reference to the drawings.

First Embodiment

[0007] Fig. 1 is a diagram that shows a layout of a DRAM cell array according to an embodiment of the invention, and Figs. 2 and 3 are cross-sectional views taken along the A-A' and B-B' lines of Fig. 1, respectively. Columnar silicon layers are formed in positions of respective memory cells MC by processing a p-type silicon substrate 1. Each memory cell MC is composed of a vertical MOS transistor formed by using the columnar silicon layer 2.

[0008] More specifically, the transistor of each memory cell MC is an NMOS transistor in which a gate electrode is formed to surround the columnar silicon layer 2 via a gate insulating film 3 and an n^+-type source diffusion layer 6 is formed at the bottom. This transistor structure is disclosed as so-called "SGT" in the paper "Impact of Surrounding Gate Transistor (SGT) for high density LSI's" by H. Takato et al. (IEEE Transactions on Electron Devices, vol. 38, No. 3, pp. 573-577, March 1991).

[0009] It is important for the source diffusion layer 6 formed at the bottom of the columnar silicon layer 2 to lie across the full extent of the bottom of the columnar silicon layer 2 to electrically insulate the p-type region of the columnar silicon layer 2 from the p-type region of the substrate 1. Thereby, in each memory cell MC, the columnar silicon layer 2 is held floating and can be controlled in bulk potential to enable dynamic recording operation by one transistor according to the invention, as explained later. In addition, the source diffusion layer 6 is formed to cover the entire surface of the substrate 1 to behave as a fixed potential line SS common to all memory cells MC.

[0010] The gate electrodes 4 surrounding the columnar silicon layer 2 are formed of a polycrystalline silicon film. By maintaining the same polycrystalline silicon film as the gate electrodes 4 continuously in one direction of the cell array, word lines (WL) 9 commonly connecting the gate electrodes 4 are formed. The surface having formed the transistors is covered by an inter-layer insulating film 7, and bit lines 8 are formed thereon. The bit lines 8 extend in the direction orthogonal to the word lines 9, and are connected to drain diffusion layers 5 of respective memory cells MC.

[0011] In this DRAM cell array, if the word lines 9 and the bit lines 8 are processed with lines and spaces of the minimum processible size F, as shown in Fig. 1, its unit cell area is $2Fx2F=4F^2$.

[0012] Fig. 4 shows a equivalent circuit of this DRAM

bit line BL (Fig. 9) when the read-out data is "0". As a result, if the data of the selected memory cell is "1", a large channel current flows and causes impact ionization, and excessive holes flow into the bulk region and have the memory write data "1" again. In case of data "0", the drain junction is forwardly biased, and holes are emitted from the bulk region and have the memory write data "0" again.

[0023] At the time t3, the word line WL is negatively biased, thereby to complete the read/refresh operations. In the other non-selected memory cells connected to the bit line BL commonly with the memory cell from which data "1" has been read out, since the word lines WL are held in negative potentials, that is, the bulk region is held in a negative potential, no channel current flows, and writing does not occur. Also in the other non-selected memory cells connected to the bit line BL commonly to the memory cell from which data "0" has been read out, the word line WL are held in negative potentials, and emission of holes does not occur.

[0024] Figs. 10 and 11 are waveforms of read/write operations of data "1" and data "0" by the same read-out system. Read-out operations at the time t1 in Figs. 10 and 11 are the same as those of Figs. 8 and 9, respectively. After reading, at the time t2, the word line WL is raised to a high potential, and in case of writing data "0" in the same selected cell, a negative potential is simultaneously applied to the bit line BL (Fig. 10). In case of writing data "1", a positive potential is applied to the bit line BL (Fig. 11). As a result, in the cell to which the data "0" is given, the drain junction is forwardly biased, and holes in the bulk region are emitted. In the cell to which the data "1" is given, a channel current flows, impact ionization occurs, and holes are accumulated in the bulk region.

[0025] As explained above, the DRAM cell according to the invention is made of SGT having the floating bulk region electrically isolated from others, and enables realization of the cell size of $4F^2$. In addition, potential control of the floating bulk region is attained by using the capacity coupling from the gate electrode, without using back gate control, and the source diffusion layer is fixed in potential as well. That is, control of read/write operations is easily accomplished only by the word line WL and the bit line BL. furthermore, since the memory cell is basically can be read in a non-destructive mode, it is not necessary to provide the sense amplifier for each bit line, and layout of the sense amplifiers is easy. Moreover, because of the current read-out system, it has a resistance to noise, and reading is possible even in the open bit line system.

[0026] In addition, by utilizing SGT using the columnar silicon layer as the memory cell, a lot of effects are obtained. In the memory cell based on the operation principle according to the invention as explained above, it is desirable that the bulk potential changes faithfully following to the word line (gate electrode). Thereby, charges accumulated in the bulk region can be held without turning on the pn junction. In normal horizontal MOS transistors, capacity between the gate electrode, i.e. the word line, and the bulk region becomes smaller as the transistor is miniaturized, and the capacity of the source and drain pn junction cannot be disregarded.

[0027] In contrast, when the SGT structure is used, since the channel region surrounds the columnar silicon layer and the channel length is determined by the height of the columnar silicon layer, a large channel length can be obtained independently from the horizontal size determined by lithography. In other words, without increasing the horizontal area, a large channel length can be realized within substantially the same area as the bit line contact. Therefore, capacity coupling between the word line and the bulk region can be increased, and reliable operation control by controlling the bulk potential from the word line is ensured.

[0028] Further, in the memory cell according to the invention, it is desirable that the threshold value change largely relative to changes of the bulk potential. This can be also realized easily by employing the SGT structure. That is, by producing a concentration profile in the substrate in its thickness direction such that the substrate impurity concentration is high in a central portion of the channel and the channel concentration near the pn junction is low, changes of the threshold value relative to changes of the bulk potential can be enlarged by the substrate biasing effect while minimizing the junction leakage. furthermore, by reducing the top area of the columnar silicon layer for contact with the bit line, the pn junction capacity connected to the bit line can be reduced, and this also contributes to relatively increasing the capacity coupling ratio of the word line and the bulk region. Further, as a result, since the bit line capacity also decreases, the charge and discharge current of the bit line capacity upon read and write operations is diminished, and higher speed and lower power consumption are attained thereby.

[0029] A concrete manufacturing process of the cell array explained with reference to Figs. 1 through 3 is next explained with reference to Figs. 12 through 17 that are cross-sectional views corresponding to the cross-sectional view of Fig. 2, showing different steps of the manufacturing process.

[0030] As shown in Fig. 12, after a buffering silicon oxide film 11 is formed to a thickness around 10 nm on a p-type silicon substrate 1, a silicon nitride film 12, approximately 200 nm thick, is formed thereon, and a resist 13 is formed and patterned thereon by lithography.

[0031] After that, as shown in Fig. 13, using the resist 13 as a mask, the silicon nitride film 12 and the silicon oxide film 11 are etched, and the silicon substrate 1 is further etched to make channels 14 extending in crossing directions and thereby form the columnar silicon layers 2. After than, the resist 13 and the silicon nitride film 12 are removed, As ions are implanted, and as shown in Fig. 14, diffusion layers 6, 5 to be used as sources and drains, respectively, are formed on tops of the chan-

ing to the instant embodiment, and Figs. 23 and 24 are cross-sectional views taken along the A-A' and B-B' lines of Fig. 22. As explained later, used as the columnar silicon layer 102 is a p-type silicon layer epitaxially grown on the silicon substrate 101. Active layer 102, which are convex silicon layers obtained by processing the p-type silicon layer, are arranged in a pattern of a grating such that each drain diffusion layer is shared by active layers 102 of different memory cells MC adjacent to each other in the bit line direction and the source diffusion layer is continuously formed in the word line direction as a common source line.

[0043] At the bottom of each active layer 102, a silicon oxide film 110 is buried. A silicon oxide film 111 is buried also in each device isolating region. Then, the gate electrode 104 is formed as a word line that lies across the active layer 102 and opposes to its three surfaces. the n^+-type source and drain diffusion layer 105 are formed in self alignment with the gate electrode 104. The surface having formed the transistors is covered with an inter-layer insulating film 106, and bit lines 107 are formed thereon.

[0044] In this manner, operation principle of the DRAM cell array using a single NMOS transistor as each memory cell MC is the same as that of the foregoing first embodiment. As already explained with the first embodiment, magnitude of the capacity coupling from the gate electrode to the floating bulk region is important for data write/read operations. Also in this embodiment, since the gate electrode 104 is opposed to three surfaces of the active layer 102 made of the columnar silicon layer, a large coupling capacity is obtained, and a favorable property is obtained.

[0045] A manufacturing process for obtaining the cell array structure according to the second embodiment is next explained with reference to Fig. 25 et seq., which show the cross section corresponding to the cross section shown in Fig. 23. As shown in Fig. 25, the silicon oxide film 110 is formed on locations of silicon substrate 101 where silicon layers should be formed later as active regions having a grating pattern, with a certain tolerance for misalignment. Thereafter, as shown in Fig. 26, a p-type silicon layer 1020 is epitaxially grown on the silicon substrate 101.

[0046] Next as shown in Fig. 27, a buffering silicon oxide film 120 and a silicon oxide film 121 are formed on the silicon layer 1020, and a resist 123 is formed and patterned thereon to cover the regions to be used as active regions by lithography. By RIE using this resist pattern 123, the silicon nitride film 121, silicon oxide film 121 and silicon layer 1020 are etched sequentially. Consecutively, the silicon oxide film 110 is etched and the exposed silicon substrate 101 is also etched to a predetermined depth.

[0047] As a result, the active layer 102 having a convex grating pattern of the p-type silicon layer 1020, which is the epitaxially grown layer, is obtained. At the bottom thereof, the silicon oxide film 110 is buried. Thereafter, by forming the silicon oxide film 111, leveling it by CMP, and processing it by etch-back using RIE, the configuration where the silicon oxide film 111 is buried approximately up to the surface level of the silicon oxide film 110 is obtained as shown in Fig. 28. The silicon oxide film 111 is used as the device isolating insulation film for isolating respective transistors in their lateral direction.

[0048] The configuration shown in Fig. 28 is illustrated in a perspective view in Fig. 30. The p-type active layer 102 is shaped into a grating pattern, and the device isolating insulation film is buried in spaces. Subsequently, as shown in Fig. 29, after the gate insulating film 103 is formed on surfaces of the p-type active layer 102 (three surfaces including the top surface and opposite side surfaces), a polycrystalline silicon film is formed and patterned to form the gate electrodes 104 which will become the word lines.

[0049] After that, as shown in Fig. 24, using the gate electrodes 104 as a mask, As ions are injected to form the source and drain diffusion layers 105. These diffusion layers 105 herein has a depth enough to reach the buried silicon oxide film 110 as shown in Fig. 24. As a result, the p-type bulk region of the transistors can be held floating to be independently controlled in potential. Thereafter, the inter-layer insulating film 106 is formed, contact holes are formed in locations thereof corresponding to the drain diffusion layers, and bit lines 107 are formed to intersect with the word lines.

Third Embodiment

[0050] Fig. 31 shows an embodiment using still another transistor structure to make up memory cells MC. On top, bottom and opposite side surfaces of an active layer 202 formed on a silicon substrate 201, a gate insulating film 203 is formed, and a gate electrode 204 is formed to lie across the active layer 202 and oppose to the top, bottom and opposite side surfaces of the active layer 202. At opposite sides of the gate electrode 204, source and drain diffusion layers are formed. Fig. 31 illustrates the active layer 202 as floating from the substrate 201. Actually, however, this structure is made by using a technique of making holes inside a silicon substrate as explained later, and the active layer 202 is not floating.

[0051] Here again, the DRAM cell array is made by using a single NMOS transistor as each memory cell MC, write and read operations of data are effected in the same manner as the first and second embodiments. Also in this case, as already explained with reference to the first embodiment, magnitude of the capacity coupling from the gate electrode to the floating bulk region is important for data write/read operations. Since the gate electrode 204 is opposed to the top and bottom surfaces of the active layer 202 mad of the columnar silicon layer, a large coupling capacity is obtained, and a favorable property is obtained.

operations according to the same principle as that of the first embodiment. Similarly to the SGT structure, since the gate electrode is formed to encircle the silicon layer and oppose to four surfaces thereof, a large gate capacity can be obtained from a small cell area, and therefore, favorable write and read characteristics are obtained.

[0062] The transistor structures according to the second and third embodiments are applicable not only to single-transistor DRAM cells but also to, in general, integrated circuits integrating transistors having a large gate capacity with a small area. In case of the third embodiment, top and bottom portions of the silicon layer are used as channels, it is possible to use only one of them as a channel. For example, a transistor using only the top wall of the void 305 as the channel can be made.

[0063] As described above, according to the invention, it is possible to provide a semiconductor memory device capable of dynamic recording of binary data with fewer signal lines by using single-transistor memory cells having a gate large capacity with a small cell area.

Claims

1. A semiconductor memory device comprising:

   a source diffusion layer formed on a semiconductor substrate and connected to a fixed potential line;
   a plurality of columnar semiconductor layers arranged in a matrix form and formed on said source diffusion layer and each having one end connected to said source diffusion layer commonly, said columnar semiconductor layer taking a first data state with a first threshold voltage that excessive majority carriers are accumulated in said columnar semiconductor layer, and a second data state with a second threshold voltage that excessive majority carriers are discharged from said columnar semiconductor layer;
   a plurality of drain diffusion layers each formed at the other end of said columnar semiconductor layer;
   a plurality of gate electrodes each opposed to said columnar semiconductor layer via a gate insulating film, and connected to said word line;
   a plurality of word lines each connected to corresponding said gate electrodes; and
   a plurality of bit lines each connected to corresponding said drain diffusion layers, said bit lines being perpendicular to said word lines.

2. The semiconductor memory device according to claim 1 wherein said source diffusion layer is made as a planar shape and commonly connects said columnar semiconductor layers arranged along said bit lines and said word lines.

3. The semiconductor memory device according to claim 1 wherein said source diffusion layer is formed to commonly connect said columnar semiconductor layers aligned along each said bit line.

4. The semiconductor memory device according to claim 1 wherein said source diffusion layer is formed to commonly connect said columnar semiconductor layers aligned along each said word line.

5. The semiconductor memory device according to claim 1 wherein each said columnar semiconductor layer is formed by processing said semiconductor substrate, and said source diffusion layer is formed at the bottom portions of said columnar semiconductor layers to keep said columnar semiconductor layers floating state where said columnar semiconductor layers are electrically isolated from said semiconductor substrate.

6. The semiconductor memory device according to claim 1 wherein said first data state is set by holding in said columnar semiconductor layer supplied with a predetermined potential from said gate electrode an excessive amount of majority carriers generated by impact ionization caused by flowing a channel current from said drain diffusion layer to said columnar semiconductor layer, and said second data state is set by discharging excessive majority carriers in said columnar semiconductor layer supplied with a predetermined potential from said gate electrode to said drain diffusion layer by applying a forward bias between said drain diffusion layer and said columnar semiconductor layer.

7. The semiconductor memory device according to claim 1 wherein said semiconductor substrate is a p-type silicon substrate.

8. The semiconductor memory device according to claim 1 wherein, upon a date write operation, said fixed potential line is set at a reference potential and wherein a first potential higher than said reference potential is applied to a selected word line, a second potential lower than said reference potential is applied to non-selected word lines, and a third potential higher than said reference potential and a fourth potential lower than said reference potential are applied to said bit lines depending upon said first and second data states, respectively.

9. The semiconductor memory device according to claim 8 wherein, upon a data read operation, a fifth potential between said first threshold voltage and said second threshold voltage and higher than said reference potential is applied to a selected word line, to detect whether a selected memory cell is in a conduction state or in a non-conduction state.

charged from said columnar semiconductor layer, comprising:

forming trenches in a semiconductor substrate in a dense alignment in a first direction and in a thin alignment in a second direction perpendicular to said first direction;

annealing said semiconductor substrate to cause surface migration and thereby close upper openings of said trenches to form voids buried in said semiconductor substrate and extending in said one direction, from corresponding said closed trenches;

forming a device isolating channels deeper than said voids in a device isolating regions of said semiconductor substrate to form active layers each having said void passing through a bottom portion thereof;

burying said device isolating grooves with device isolating layers to a depth not closing both ends of said voids;

forming gate insulating films each including a first insulating film on surface of said active layer and second insulating film on the inner wall surface of said void;

forming gate electrodes such that each said gate electrode includes a first portion and a second portion, said first and second portions extending in other direction perpendicular to said one direction, said first and second portions being formed to cross said active layer, said first portion being on said first insulating film and said second portion being on said second insulating film, said first and second portions being connected to each other at end portions thereof; and

forming source and drain diffusion layers in said active layer in self alignment with said gate electrode.

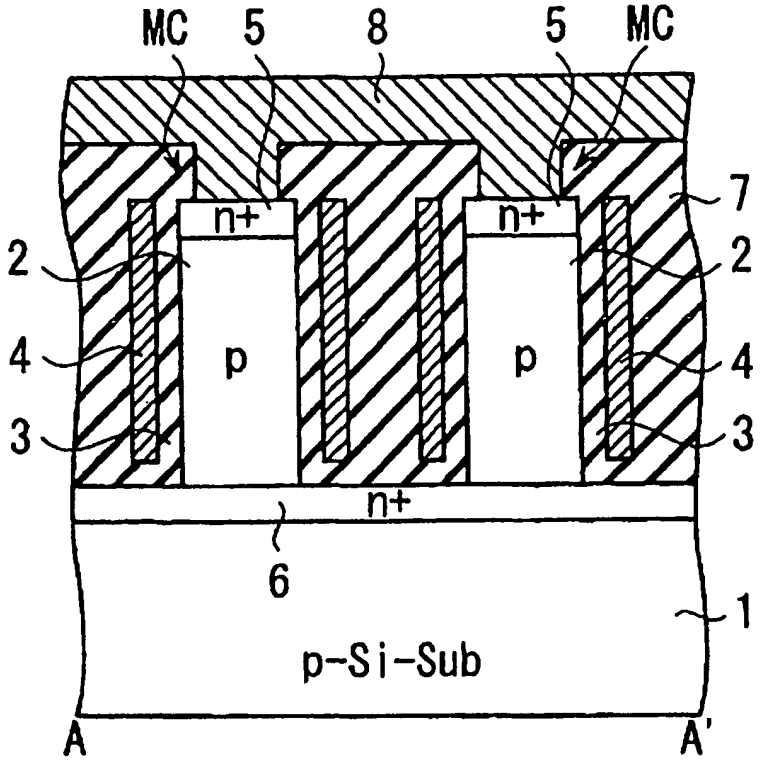

FIG. 2

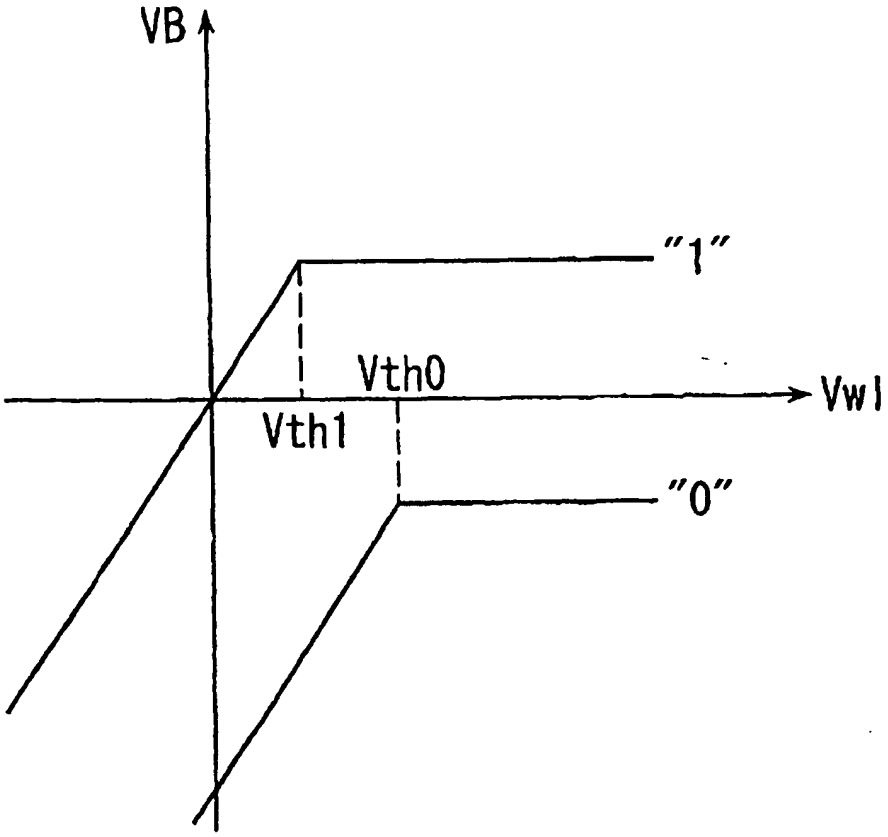

FIG. 5

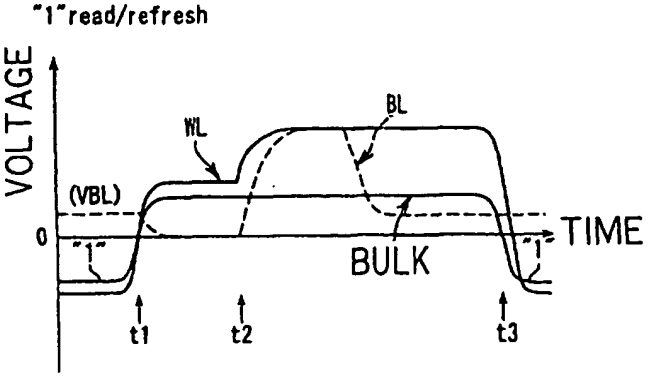

FIG. 8

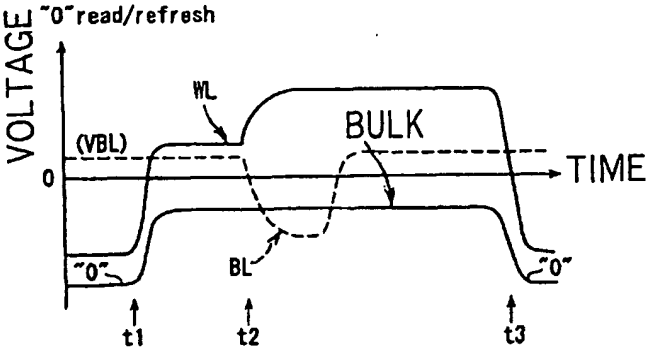

FIG. 9

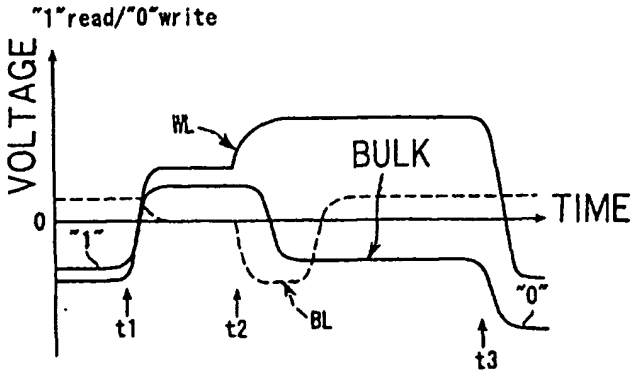

FIG. 10

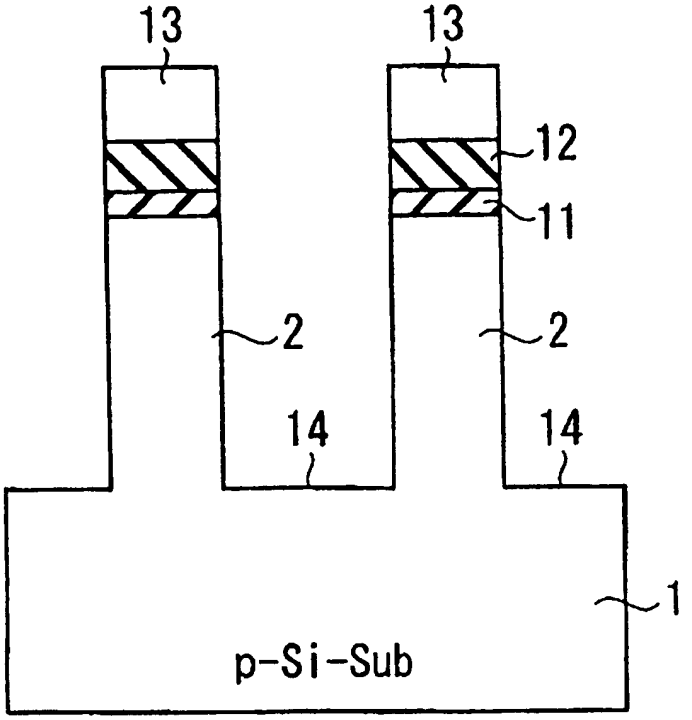

FIG. 13

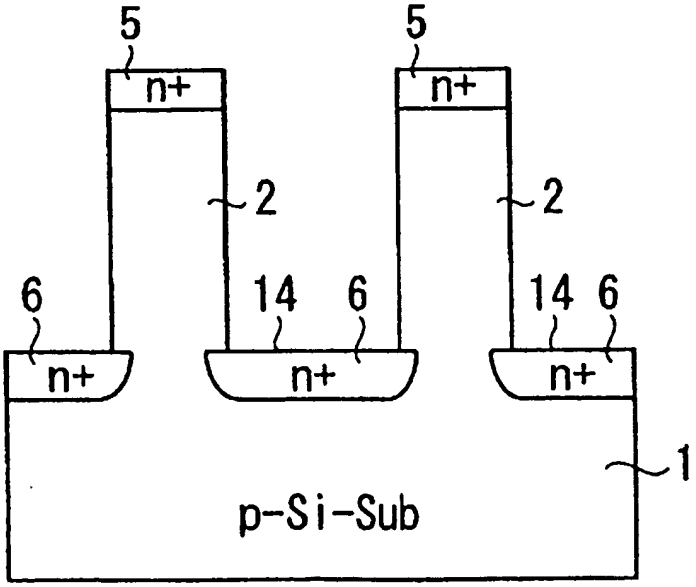

FIG. 14

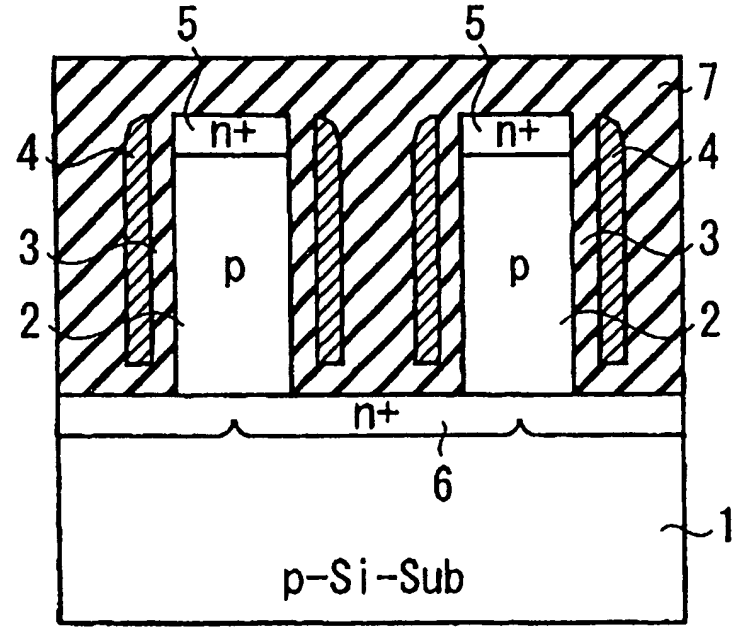

FIG. 17

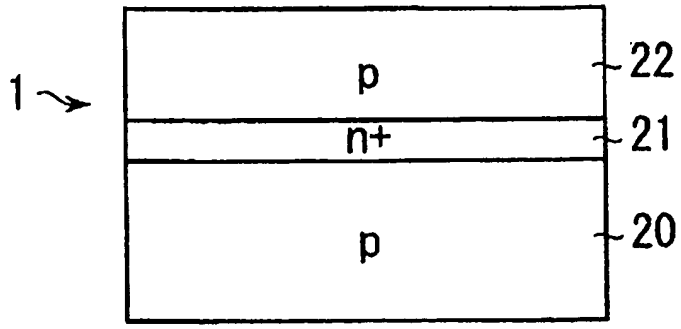

FIG. 18

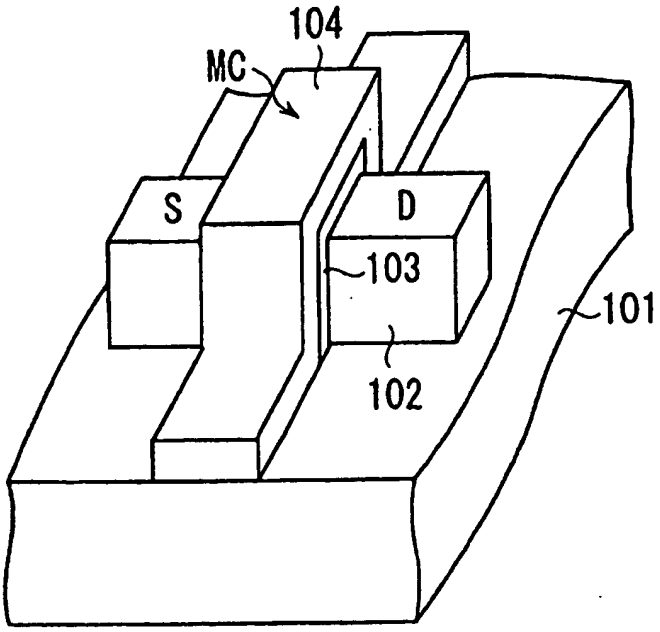
104
MC
S
D
103
101
102

FIG. 21

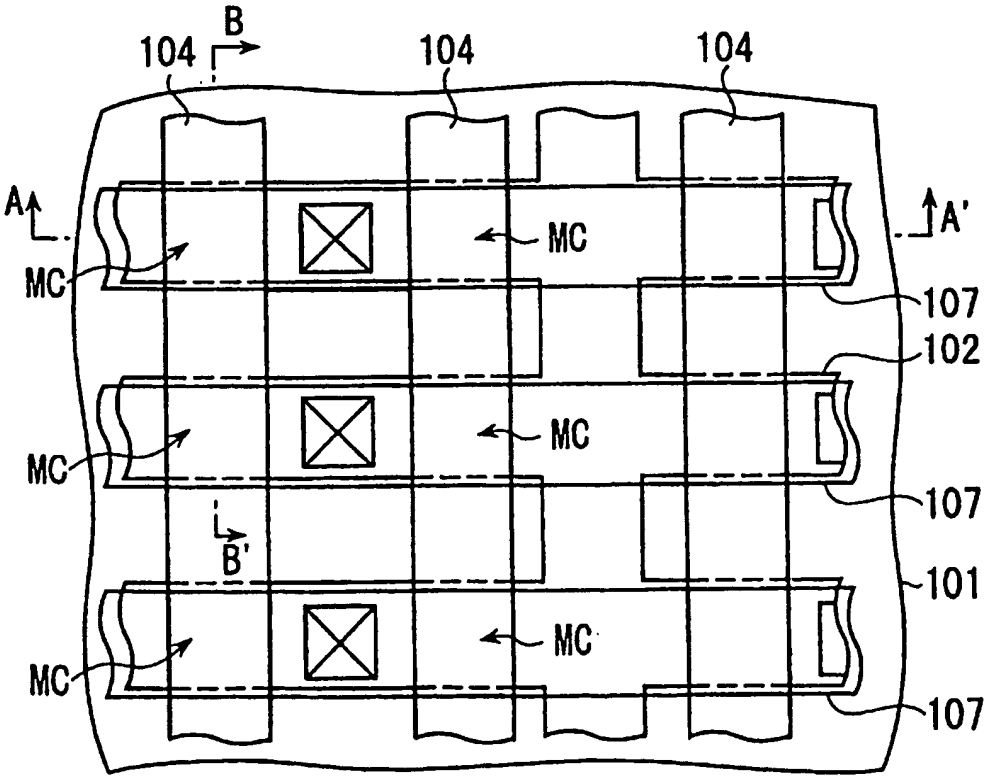
B
104
104
104
A
A'
MC
MC
107
102
MC
MC
107
B'
101
MC
MC
107

FIG. 22

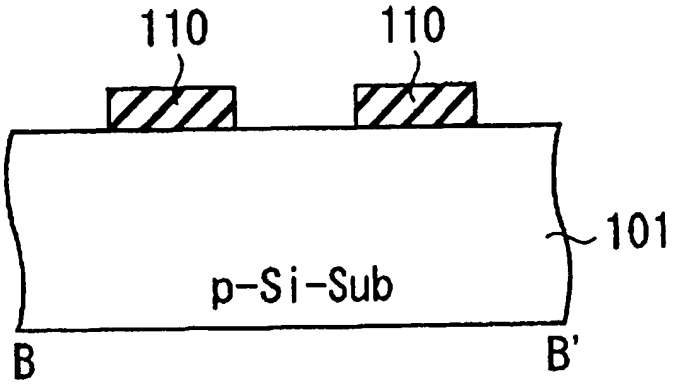

FIG. 25

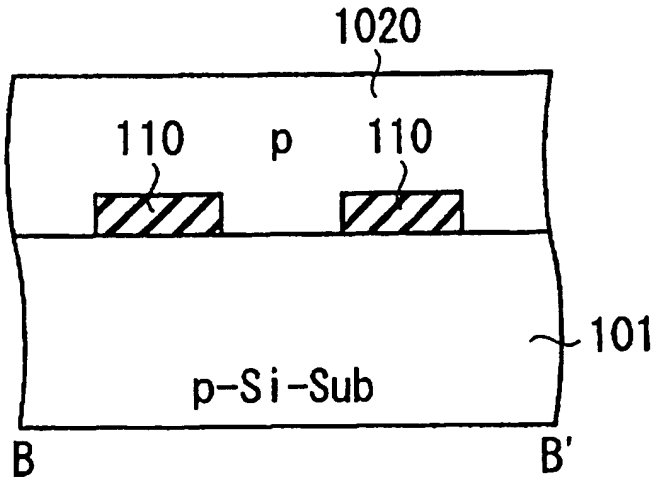

FIG. 26

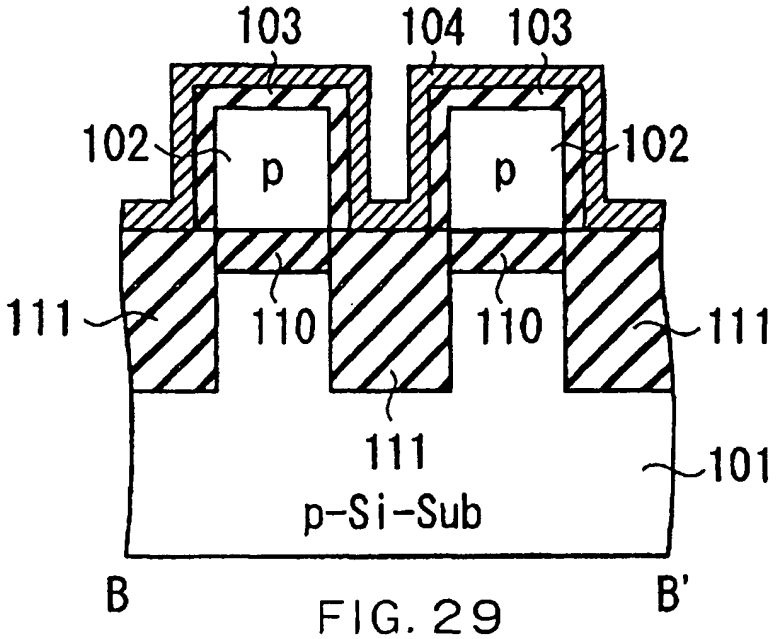
103
104
103
102
p
p
102
111
110
110
111
111
101
p-Si-Sub
B
B'

FIG. 29

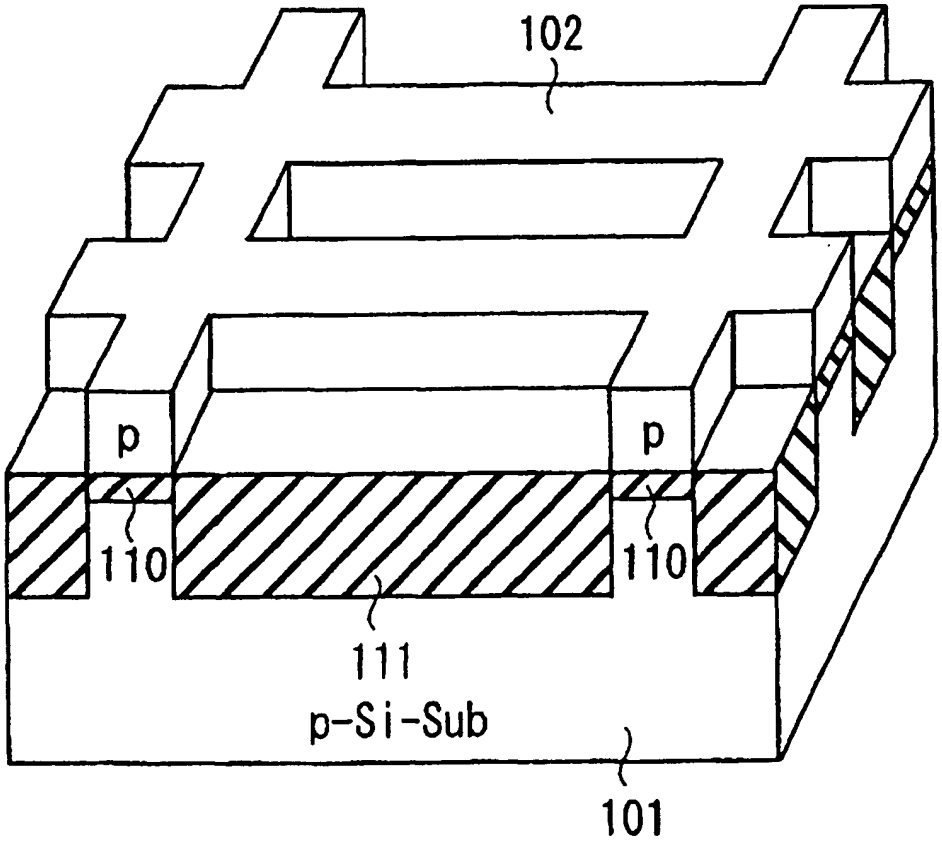
102
p
p
110
110
111
p-Si-Sub
101

FIG. 30

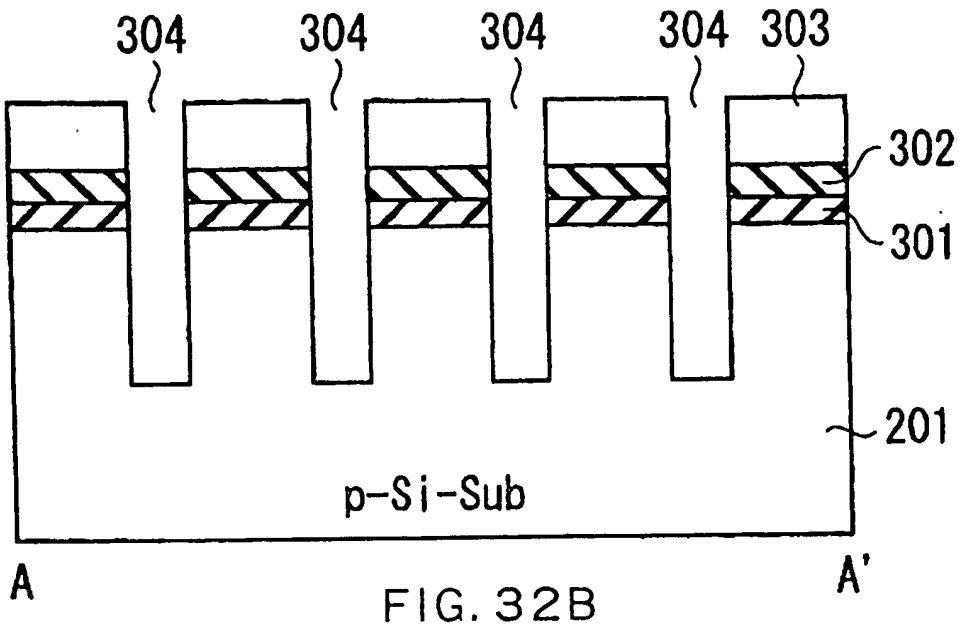

FIG. 32B

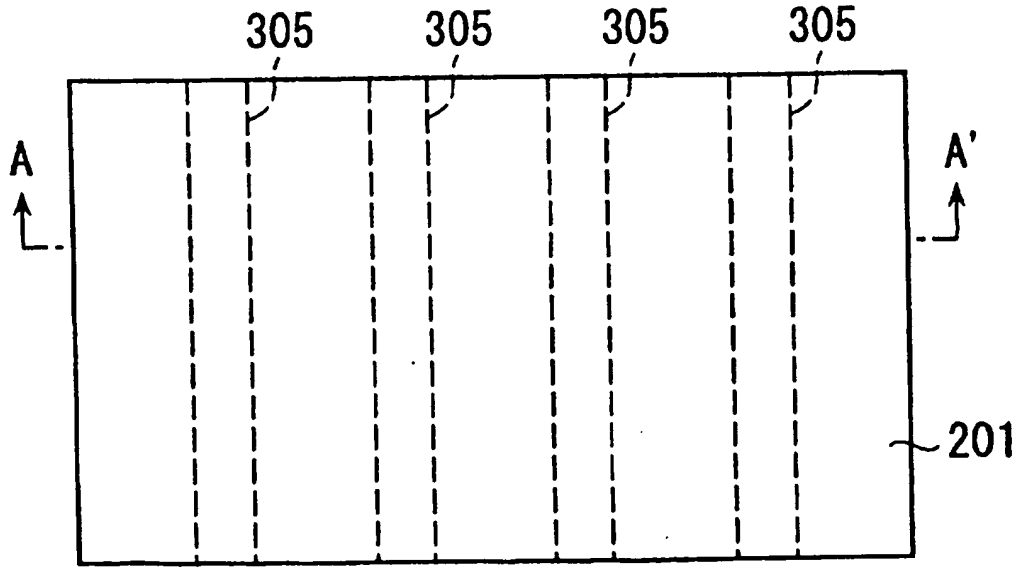

FIG. 33A

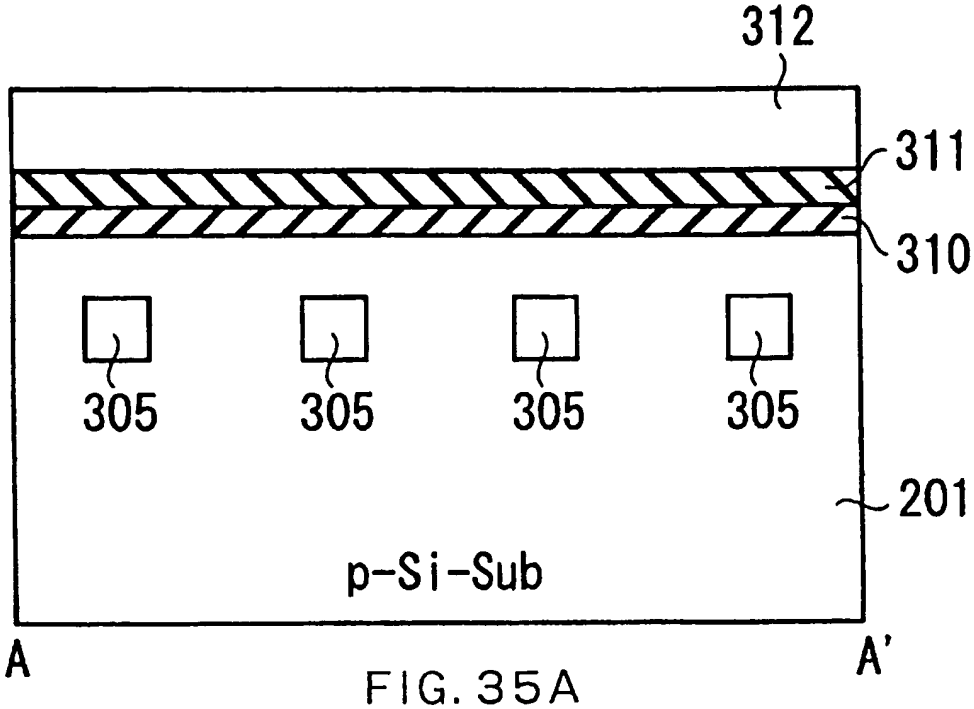

FIG. 35A

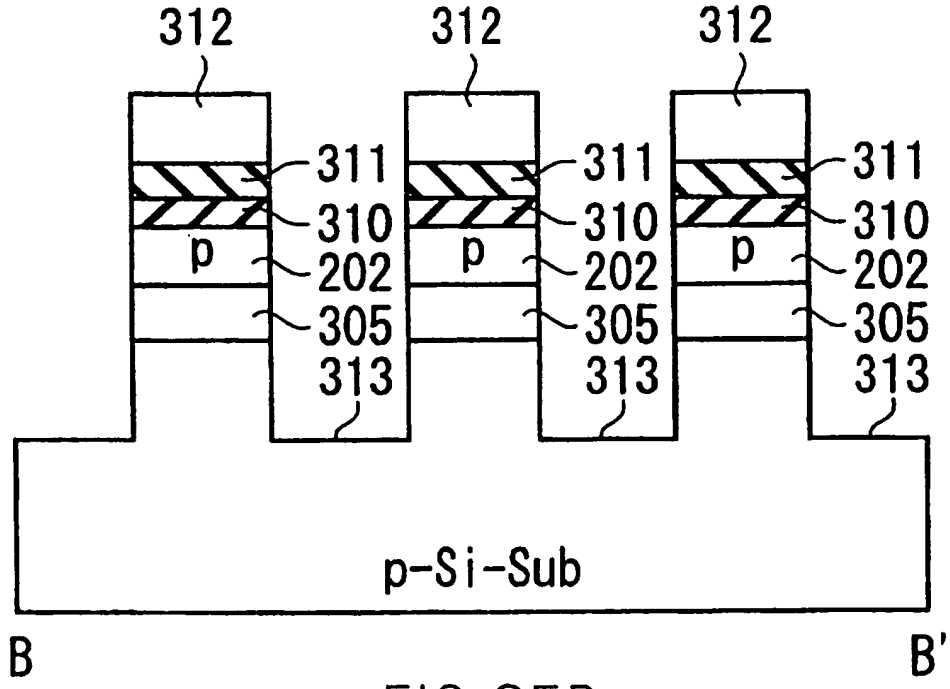

FIG. 35B

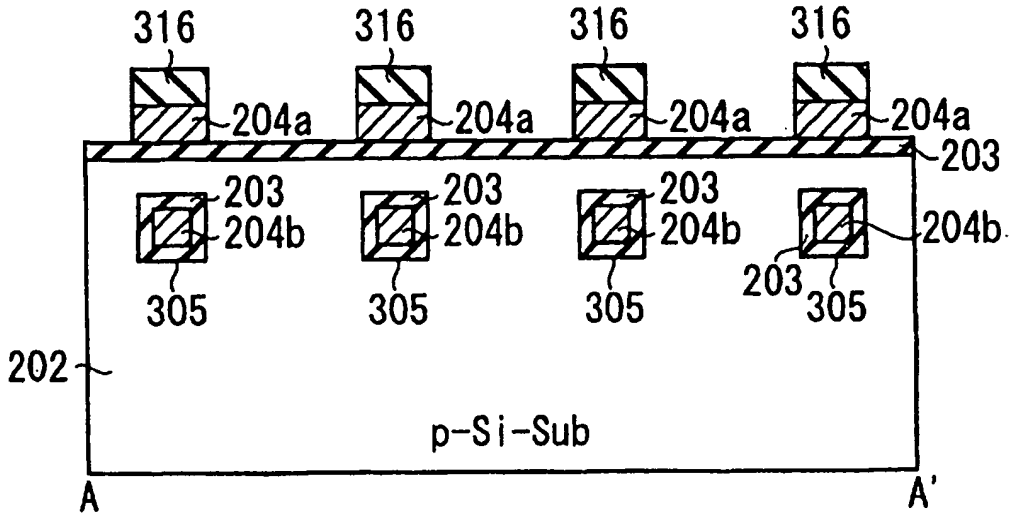

FIG. 37A

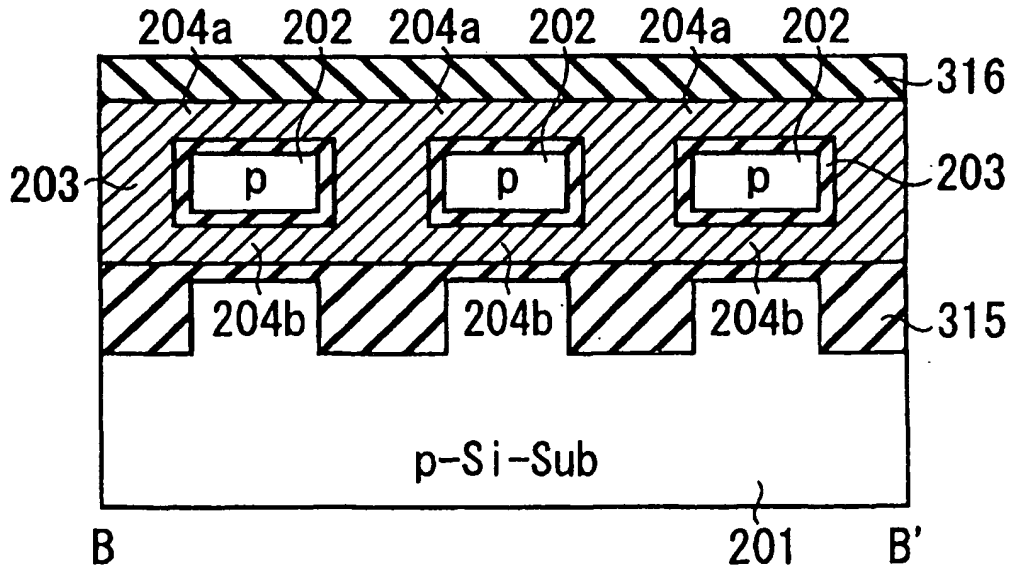

FIG. 37B

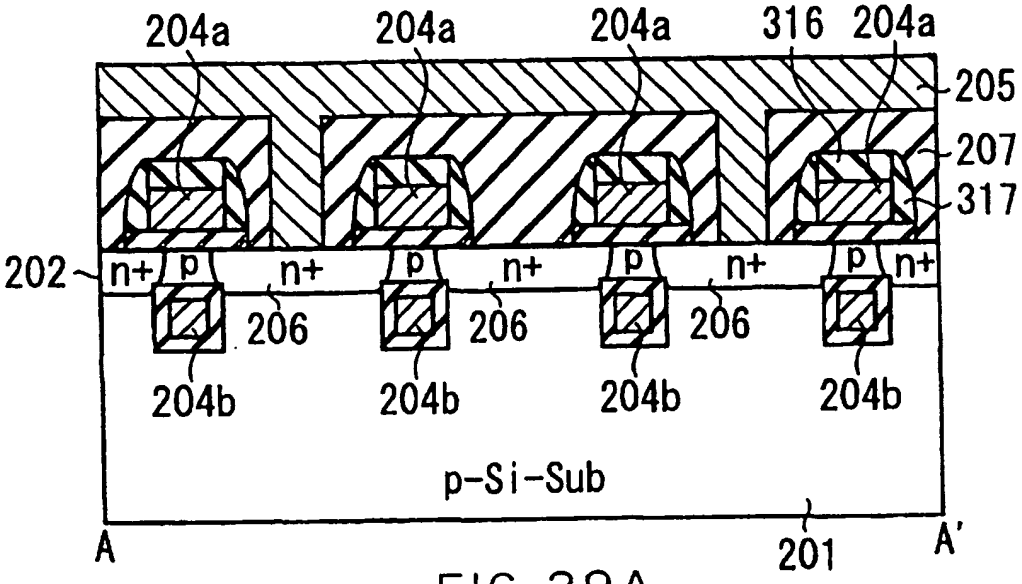

FIG. 39A

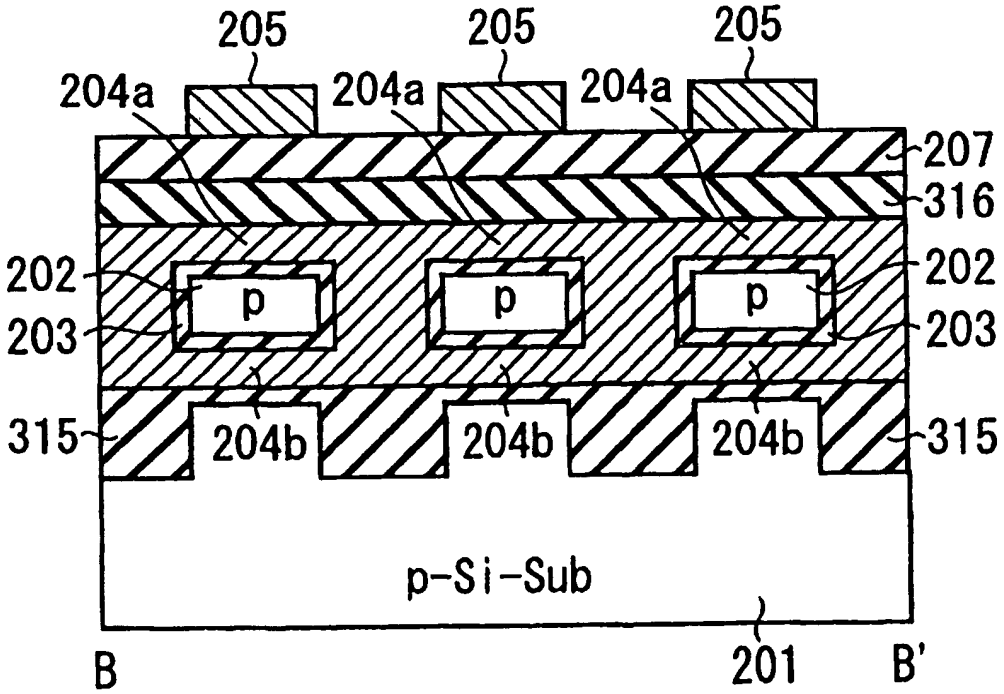

FIG. 39B